REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action mailed February 14, 2001, and hereby respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-43 in the application. In response to a restriction requirement, the Applicants elected Claims 1-10 without traverse. The Applicants have amended Claim 1 in the present amendment. Accordingly, Claims 1-10 are currently pending in the application.

I. Rejections of Claims 1-2 and 4-9 under 35 U.S.C. §102

The Examiner has rejected Claims 1-2 and 4-9 under 35 U.S.C. §102(b), as being anticipated by U.S. Patent No. 5,326,991 to Takasu. As the Examiner is no doubt aware, anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention. Furthermore, anticipation requires the presence, in the single prior art reference, of all elements of a claimed invention arranged as in the rejected claims.

Takasu discloses a semiconductor device with a silicon carbide layer uniform in plane bearing and isolated from the silicon substrate by an insulating layer. The silicon carbide layer is grown epitaxially through openings in a silicon dioxide layer to form a seed crystal layer. (Abstract). The silicon substrate is then oxidized under the openings with the silicon carbide seed crystal layer used as a barrier, thereby cutting off the connection between the silicon carbide seed crystal layer and the silicon substrate. (Column 2, lines 34-38). The seed crystal layer is then

epitaxially grown to form a silicon carbide layer with regions isolated from one another and the substrate. Within the isolated regions of the silicon carbide layer, metal oxide semiconductor devices are formed. (Abstract).

The present application relates to a silicon carbide metal oxide semiconductor field effect transistor (SiC MOSFET) having high breakdown voltage. (Page 1, lines 5-7). The silicon carbide layer of the lateral MOSFET is located on or within a substrate of a semiconductor wafer. (Claim 1). As an example, the silicon carbide layer is formed on the substrate by growing a cubic crystalline silicon carbide in the presence of a P-type dopant. (Page 14, lines 21-23 and Figure 2A). In another example, the silicon carbide layer is located within the substrate by forming a silicon trench in the substrate prior to the formation of the silicon carbide layer. The silicon carbide layer is then deposited in the silicon trench. (Page 16, lines 19-22 and Figure 2F).

Takasu, however, fails to disclose a silicon carbide layer located on or within a substrate as recited in Claim 1 of the present application. As a matter of fact, the silicon carbide layer of Takasu is clearly insulated from the underlying substrate. Thus, not only does Takasu not disclose the invention of Claim 1, but there is no suggestion or identifiable motivation to modify the semiconductor device of Takasu to arrive at the claimed invention.

Takasu, therefore, does not disclose, or even suggest, each and every element of Claim 1 and, as such, is not an anticipating reference. Because Claims 2 and 4-9 are dependent upon Claim 1, Takasu also cannot be an anticipating reference for Claims 2 and 4-9. Accordingly, the Applicants respectfully request the Examiner withdraw the §102 rejection with respect to these Claims.

II. Rejection of Claims 1-10 under 35 U.S.C. §103

The Examiner has rejected Claims 1-10 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,326,991 to Takasu. The Examiner suggests that it would have been obvious at the time of the invention to use the MOSFET structure of Takasu as a power switch employed in a power train of a power converter. It appears that the Examiner is directing the comments to dependent Claim 10 of the present application. The Examiner then takes judicial notice that it is known in the art that a silicon carbide layer has a breakdown voltage of at least about 10 volts as recited in dependent Claim 3 of the present application. Thus, the Examiner believes that Takasu anticipates the entire claimed structure of independent Claim 1 and employs Takasu under 35 U.S.C. §103(a) primarily in connection with subject matter disclosed in dependent claims of the present application.

As discussed above, however, Takasu fails to teach or suggest all of the elements of the invention recited in independent Claim 1. Since Takasu fails to teach or suggest all of the elements of Claim 1, the Examiner cannot establish a *prima facie* case of obviousness of dependent Claims 2-10 which include all the elements of independent Claim 1. Therefore the claimed invention is not obvious in view of the foregoing reference, and the Examiner has failed to establish a *prima facie* case of obviousness of dependent Claims 2-10. The Applicants, therefore, have overcome the Examiner's rejection of Claims 1-10 under 35 U.S.C. §103(a), and respectfully request the Examiner withdraw the rejection of these claims.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-10.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

1. The title of the invention on the cover page, page 1 and page 33 has been amended as follows:

SiC [NMOSFET] MOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME

2. The paragraph beginning at page 5, line 13 has been amended as follows:

In another embodiment, the MOSFET further includes a buried oxide layer[. The buried oxide layer may be formed in the substrate. However, in one advantageous embodiment, it is] that may be formed in the substrate. The gate and substrate may be comprised of conventional materials, such as poly-silicon and silicon, respectfully. In those embodiments where the silicon carbide is formed on a silicon substrate, a 3C silicon carbide structure is formed. In yet another embodiment, the MOSFET is formed on a semiconductor wafer that includes a CMOS device, which, in certain embodiments, may form a drive controller for a power converter.

3. The paragraph beginning at page 6, line 13, has been amended as follows:

As was the case with the device, the method may also comprise forming a buried oxide layer in the substrate.[However, in preferred embodiments, the buried oxide layer is formed in the

substrate.] Moreover, forming source and drain regions may comprise implanting an N-type dopant into the silicon carbide layer, which may be doped with a P-type dopant.

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Amended) A lateral metal-oxide semiconductor field effect transistor (MOSFET), comprising:

a silicon carbide layer located [over] on or within a substrate of a semiconductor wafer, a gate formed on the silicon carbide layer; and

source and drain regions located in the silicon carbide layer and laterally offset from the gate.